Japanese Patent Laid-Open No. 6-333824

Laid-Open Date: December 2, 1994

Application No. 5-142880

Application Date: May 21, 1993

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[Title of the Invention]

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

[Abstract]

[Purpose] To reduce the effects of metallic elements in a crystalline silicon film.

[Constitution] A PSG film 99 is formed on a substrate 101 and an insulating film 102 is formed thereon and an amorphous silicon film 104 is formed thereon and metallic elements are introduced into a region 100, and then the amorphous silicon film 104 is crystallized at a temperature of 600 °C or less by using the metallic elements as a catalytic material. At this time, the gettering of the metallic elements is achieved by the action of the PSG film 99, whereby the effects of the metallic elements are reduced.

[Claims]

[Claim 1] A semiconductor device comprising:

a PSG film formed over a substrate;

an insulating film formed over the PSG film; and

a crystalline silicon film formed over the insulating film;

wherein metallic elements for facilitating the crystallization of the crystalline silicon film are included in the crystalline silicon film.

[Claim 2] A semiconductor device as claimed in claim 1, wherein the metallic element is at least one selected from the group consisting of nickel, cobalt, iron, and platinum.

[Claim 3] A method of manufacturing a semiconductor device, said method comprising the steps of:

forming a PSG film over a substrate;

forming an insulating film as an underlayer film over the PSG film;

forming a substantially amorphous silicon film over the underlayer film;

introducing into the silicon film at least one selected from the group consisting of nickel, cobalt, iron, and platinum; and

annealing the silicon film at a temperature lower than the crystallization temperature of a usual amorphous silicon film to crystallize the silicon film in the region into which at least one selected from the group consisting of nickel, cobalt, iron, and platinum is introduced.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention] The present invention relates to a method of utilizing a crystalline silicon film crystallized by heating and annealing an amorphous silicon film for a semiconductor device.

[0002]

[Description of the Prior Art] An active matrix type liquid crystal display device has been known in which many TFTs (thin film transistor: in general, insulating gate type field effect semiconductor using a thin film silicon semiconductor is used) are formed on a glass substrate in a shape of matrix and drive pixels arranged also in a shape of matrix. As the TFT used for driving the pixels of the active matrix type liquid crystal display device, a TFT using amorphous silicon is usually used. However, in order to improve performance, it is effective to use silicon having crystallization (hereinafter referred to as crystalline silicon).

[0003]

A method of giving the energy of laser light to amorphous silicon formed by a vapor phase method or a sputtering method to crystallize the amorphous silicon, and a method of heating and annealing amorphous silicon formed by the vapor phase method or the sputtering method to crystallize the amorphous silicon have been known as methods of forming crystalline silicon. However, the method using the laser light is

impractical, because the irradiation area of the laser light is small and there is a problem in reproducibility. Also, the method of heating and annealing needs a heating temperature of 600 °C or more and hence when a glass substrate is used as a substrate (in general, coning 7059 glass is used), the temperature of 600 °C is a little high for the glass (because the coning 7059 glass has a distortion point of 593 °C) and hence this method is inappropriate for a large area substrate. Further, in this method, it is necessary to heat and anneal the substrate at a temperature of 600 °C for about 24 hours, and this is a problem from the viewpoint of productivity.

[0004]

On the other hand, the following fact was verified by experiment: if a small amount of nickel element is introduced into the amorphous silicon film and then the amorphous silicon film is heated and annealed at 550 °C for about 4 hours, the amorphous silicon film is crystallized. However, in this method of facilitating crystallization by heating and annealing by using the nickel as a catalytic material, the metallic element nickel remains in the crystalline silicon, and hence when a semiconductor device (for example, TFT) is manufactured by using this crystalline silicon, there is apprehension that the performance or the reliability of the semiconductor device might be reduced.

[0005]

[Problems to be solved by the Invention] Therefore, it is the object of the present invention to provide a method of reducing the effect of a metallic element which is a catalytic material for crystallization and remains in the crystalline silicon film in a method of forming crystalline silicon on a glass substrate by annealing at a temperature of about 550 °C (in experiment, crystallization was observed at a temperature of about 450 °C).

[0006]

[Means for Solving the Problems](First invention) The aspect of the first invention, as claimed in claim 1, is a semiconductor device including a PSG film formed on a substrate, an insulating film formed on the PSG film, and a crystalline silicon film formed on the insulating film,

wherein metallic elements for facilitating the crystallization of the crystalline silicon film are included in the crystalline silicon film.

[0007]

The first invention described above makes the PSG film formed on the substrate perform the gettering of the metallic elements which are introduced thereinto as a catalytic material so as to facilitate crystallization and remain in the crystalline silicon film. In the invention described above, the PSG film means Phosphosilicate Glass, and as is well known, can be formed by a coating method or a vapor phase method.

[0008]

As the metallic element of the catalytic material for facilitating the crystallization of the silicon film, at least one selected from the group consisting of nickel, iron, cobalt, and platinum can be used.

[0009]

(Third invention) The aspect of the third invention is, as claimed in claim 3, a method of manufacturing a semiconductor device, the method including the steps of: forming a PSG film over a substrate; forming an insulating film as an underlayer film over the PSG film; forming a substantially amorphous silicon film over the underlayer film; introducing into the silicon film at least one selected from the group consisting of nickel, cobalt, iron, and platinum; and annealing the silicon film at a temperature lower than the crystallization temperature of a usual amorphous silicon film to crystallize the silicon film in the region into which at least one selected from the group consisting of nickel, iron, cobalt, and platinum is introduced.

[0010]

The third invention described above is a manufacturing process for achieving the first invention. In the third invention described above, as a method of manufacturing a substantially amorphous silicon film, a plasma CVD method, a low pressure thermal CVD method, a photo CVD method, or a

sputtering method, each of which is well-known, can be used. The substantially amorphous silicon film means an amorphous silicon semiconductor film used for an amorphous silicon solar cell and an amorphous silicon TFT.

[0011]

The crystallization temperature of the usual amorphous silicon film means a temperature of 600 °C or more, as described above. That is, the present invention is characterized in that the amorphous silicon film can be crystallized at a temperature of 600 °C or less. It is verified that the crystallization process in accordance with the present invention is fully completed for about 4 hours if the temperature is 550 °C and can be completed even if the temperature is about 450 °C. Therefore, it can be determined that the annealing temperature for crystallization in accordance with the present invention ranges from 450 °C to 550 °C (of course, the temperature may be increased, if the heat resistance of the substrate permits).

[0012]

[Operation of the Invention] The PSG film can perform the gettering of the metallic element such as nickel which acts as a catalyst when the silicon film is crystallized, and can improve the electric characteristics and the stability of the semiconductor device utilizing the crystallized silicon film.

[0013]

[Embodiment of the Invention](Embodiment 1) The present

embodiment is an example of forming on a glass substrate a circuit in which a P-channel type TFT (referred to as a PTFT) an N-channel type TFT (referred to as an NTFT) both of which are made of crystalline silicon are combined with each other in a complementary type. The constitution of the present embodiment can be utilized for a peripheral driver circuit of an active liquid crystal display device and a switching element of a pixel part thereof (for driving a pixel by a complementary circuit)

[0014]

FIG. 1 illustrates cross-sectional views of a manufacturing process of the present embodiment. First, on a substrate (coning 7059) 101, a PSG film 99 was formed to a thickness of 1000 Å by a spin-coating method, and was subjected to a baking process at 200 °C, whereby a film forming process was finished. As a material for the PSG film 99, a commercially available silicon oxide film base coating liquid for forming a film was used, and the concentration of P was set at 5×10^{14} cm^{-3} to 5×10^{21} cm^{-3} . It is recommended that the thickness of the PSG film 99 be within a range from 200 Å to 2000 Å.

[0015]

Then, an underlayer film 102 made of silicon oxide was formed to a thickness of 100 Å to 2000 Å, here 500 Å. It is effective for improving a gettering effect to add chlorine

to the underlayer film 102. Then, an intrinsic (I-type) amorphous silicon film 104 having a thickness of 500 Å to 1500 Å, for example, 1000 Å, was deposited by a plasma CVD method. Then, there was provided a mask 103 constituted by a metal mask, silicon oxide film, or the like. The mask 103 exposes the amorphous silicon film 104 in a shape of slit. That is, when a state in FIG. 1(A) is viewed from the top, the silicon film 104 is exposed in a shape of slit and the other portion is masked.

[0016]

After the mask 103 was provided, a nickel silicide film (chemical formula, $NiSi_x$, $0.4 \leqq x \leqq 2.5$, for example $x = 2.0$) having a thickness of 5 Å to 200 Å, for example, 20 Å, was formed by a sputtering method. By this process, the nickel silicide film was selectively introduced into a region 100 on the silicon film 104.

[0017]

Then, the mask 103 was removed and then the nickel silicide film was annealed in a reducing atmosphere by hydrogen (preferably, the partial pressure of hydrogen is 0.1 atmospheric pressure to 1.0 atmospheric pressure) at 550 °C for 4 hours, thereby being crystallized. At this time, in the region 100 where the nickel silicide film was selectively formed, the silicon film 104 was crystallized in a vertical direction with respect to the substrate 101. And in the region other than the region 100, as shown by an arrow 105, the silicon

film 104 was crystallized in the lateral direction (in the direction parallel to the substrate 101) from the region 100.

[0018]

As a result of the process described above, the amorphous silicon film was crystallized to produce a crystalline silicon film 104. Then, the crystalline silicon film 104 was patterned to separate elements. Then, a silicon oxide film 106 having a thickness of 1000 Å was deposited as a gate insulating film by the sputtering method. A sputtering process was performed under the following conditions: silicon oxide was used as a target; the temperature of the substrate was 200 °C to 400 °C, for example, 350 °C; and a sputtering atmosphere included oxygen and argon, a ratio of argon/ oxygen being 0 to 0.5, for example, 0.1 or less. Then, aluminum (including 0.1 % to 2 % silicon) having a thickness of 6000 Å to 8000 Å, for example, 6000 Å, was deposited by the sputtering method. In this regard, it is desirable that the processes for forming the silicon oxide film 106 and the aluminum film are performed in succession.

[0019]

Then, the silicon film was patterned to form gate electrodes 107, and 109. Then, the surface of the aluminum electrode is anode-oxidized to form oxide layers 108 and 110 on the surface thereof. The anode oxidation was performed in an ethyleneglycol solution including 1 % to 5 % tartaric acid. The thickness of the obtained oxide layers 108 and 110 was 2000

Å. In this regard, since the oxide layers 108, 110 become a thickness for forming an offset gate region in a following ion doping process, the length of the offset gate region can be determined in the anodic oxidation process described above.

[0020]

Then, impurities (phosphorus and boron) were implanted into the silicon region by an ion doping method by using the gate electrode 107 and the oxide layer 108 around it, and the gate electrode 109 and the oxide layer 110 around it as masks. As a doping gas, a phosphine gas (PH_3) and a diboron gas (B_2H_6) were used, and an acceleration voltage was set at 60 kV to 90 kV, for example, 80 kV for the former gas and at 40 kV to 80 kV, for example, 65 kV for the latter gas. The amount of doping was set at 1×10^{15} cm^{-2} to 8×10^{15} cm^{-2}, for example, the amount of phosphorus was set at 2×10^{15} cm^{-2} and the amount of boron was set at 5×10^{15} cm^{-2}. When the silicon region was doped with the element, it was selectively doped with each element in the region requiring the element by covering the other region with a photoresist. As a result of this, N-type impurity regions 114 and 116 and P-type impurity regions 111 and 113 were formed and hence a P-channel type TFT (PTFT) and an N-channel type TFT (NTFT) could be formed.

[0021]

Then, annealing was performed by the irradiation of laser light. As the laser light, a KrF excimer laser

be used. The irradiation conditions of the laser light were as follows: energy density was set at 200 mJ/ cm^2 to 400 mJ/ cm^2 , for example, 250 mJ/ cm^2, and 2 shots to 10 shots per one position, for example, 2 shots per one position. It is useful to heat the substrate to a temperature of about 200 °C to about 450 °C when the substrate is irradiated with the laser light. In this laser annealing process, since nickel was diffused in the previously crystallized region, the irradiation of the laser light facilitated recrystallization easily and could easily activate the impurity regions 111 and 113 doped with impurities for producing a P-type and the impurity regions 114 and 116 doped with impurities for producing an N-type.

[0022]

Then, a silicon oxide film 118 having a thickness of 6000 Å was formed as an interlayer insulating material by the plasma CVD method, and a contact hole was made therein, and the electrodes and the wirings 117, 120, 119 of the TFT were formed by the multilayer film made of metallic materials, for example, titanium nitride and aluminum. Last, annealing was performed in a hydrogen atmosphere at 1 atmospheric pressure at a temperature of 350 °C for 30 minutes. A semiconductor circuit was completed by the processes described above (FIG. 1 (D)). This circuit has a complementary constitution in which the gate electrode is an input and the electrode 120 is an output.

[0023]

the gate electrode is an input and the electrode 120 is an output.

[0023]

The circuit described above has a CMOS structure in which the PTFT and the NTFT are provided in a complementary type, but it is also possible to form two independent TFTs at the same time by forming two TFTs at the same time and then by severing them at the center.

[0024]

FIG. 2 is a schematic view when FIG. 1 (D) is viewed from the top. The Ni addition region in FIG. 2 is the region 100 shown in FIG. 1 (A). Also, the gate electrodes correspond to 107, 109, the source/ drain regions correspond to 111 and 116, and the drain/ source regions correspond to 113 and 114. Also, in FIG. 2, the gate insulating film and the channel forming regions are formed under the gate electrode. As is evident from FIG. 2, by elongating the Ni addition region further (in FIG. 2, elongating it in up-and-down direction), a plurality of TFTs can be produced at the same time.

[0025]

In the present embodiment, as a method of introducing nickel, a method was adopted in which a nickel thin film was formed selectively on the amorphous silicon film 104 (the film was extremely thin and hence it was difficult to observe the film) and then the crystal growth was achieved from this portion.

However, it is also possible to use a method of forming a nickel silicide film selectively before forming the amorphous silicon film 104. That is, the crystal may be grown from the top surface of the amorphous silicon film or from the bottom surface thereof. Further, it is also possible to use a method of forming the amorphous silicon film 104 in advance and then implanting nickel ions selectively into the amorphous silicon film 104 by the ion doping method. This method has an advantage of controlling the concentration of the nickel element.

[0026]

In this regard, in the present embodiment, the nickel concentration of the crystalline silicon measured with a SIMS (Secondary Ion Mass Spectrometric Analysis) was 10^{17} cm^3 to 10^{18} cm^3.

[0027]

(Embodiment 2) This embodiment is an example of an active liquid crystal display device in which each pixel is provided with an N-type TFT as a switching element. One pixel will be described below and the other many pixels (in general, hundreds of thousands of pixels) were formed in the similar structure.

[0028]

The schematic manufacturing process of the present embodiment will be shown in FIG. 3. In the present embodiment, a coning 7059 glass substrate (thickness: 1.1 mm, 300 × 400 mm) was used as a transparent insulating substrate 301. As

is the case with the embodiment 1, a PSG film 302 was applied to the glass substrate to a thickness of 200 Å to 2000 Å, here 1000 Å, by the spin-coating method, and then was subjected to a baking process at 200 °C for 30 minutes. Then, an underlayer film 303 (silicon oxide) was formed to a thickness of 500 Å by the sputtering method.

[0029]

Then, an amorphous silicon film 304 (thickness of 300 Å to 1500 Å, here 1000 Å) was formed by an LPCVD method or the plasma CVD method, and then a nickel silicide film was formed. The nickel silicide film was formed to a thickness of 5 Å to 200 Å, for example, 20 Å by the sputtering method. The nickel silicide film is expressed by a chemical formula of $NiSi_x$, where $0.4 \leqq x \leqq 2.5$, for example, $x = 2.0$. That is, in the constitution of the present embodiment, as shown in FIG. 3 (B), the amorphous silicon film 304 was formed, and then onto the surface thereof, nickel was introduced as a nickel silicide film.

[0030]

Then, the film was dehydrogenated at 400 °C for 1 hour and then was crystallized by heating and annealing. The annealing process was performed in a reducing atmosphere by hydrogen (preferably, the partial pressure of hydrogen is 0.1 to 1.0 atmospheric pressure) at 550 °C for 4 hours. In this regard, since the nickel silicide film was formed on the

amorphous silicon film 304, the nickel silicide film was crystallized in the vertical direction with respect to the substrate 301. A crystalline silicon film could be obtained whose crystal was grown in the vertical direction with respect to the substrate 301.

[0031]

An island-shaped semiconductor region (TFT active layer) was formed by patterning (separating the elements of) the semiconductor region (a portion shown by 304) made of this crystalline silicon. Then, a gate insulating film made of silicon oxide 305 (thickness of 700 Å to 1200 Å, typically, 1000 Å) was formed by the plasma CVD method in an oxygen atmosphere by using tetraethoxysilane (TEOS) as a raw material. The temperature of the substrate was set at 400 °C or less, preferably, 200 °C to 350 °C so as to prevent the glass from being contracted or warped. However, a lot of hydrocarbon groups were included in the oxide film at this temperature of the substrate and many recombination centers existed, for example, at an interfacial level density of 10^{12} cm^{-2} or more, which is a level of incapable of being used as the gate insulating film.

[0032]

Therefore, by applying KrF laser light, the crystallization of the crystalline silicon film 304 was facilitated and the recombination centers (trap centers) of

the gate oxide film 305 were reduced to improve the characteristics of the gate insulating film 305. Further, preferably, the laser is applied at a reduced pressure of 10 Torr or less. This is because carbon atoms are relieved more easily from the oxide film under the reduced pressure. At this time, the energy density of the laser light was set at 250 mJ/ cm^2 to 300 mJ/ cm^2 , and the number of shots was set at 10 shots. In this respect, it is recommended that the temperature of the substrate be kept at 200 °C to 400 °C, typically, at 300 °C. As a result, the crystallization of the silicon film 204 could be improved and the interfacial level density of the gate oxide film was reduced to 10^{11} cm^{-2} or less.

[0033]

Then, an aluminum gate electrode 306 was formed and each substrate was dipped in an electrolytic solution and a current is passed therethrough by using the gate electrode 306 as an anode to form an anode oxide layer 314 having a thickness of 2000 Å on the surfaces of the aluminum wirings of the gate electrode and the like. A state in which this process was finished will be shown in FIG. 3 (C). Also, it is recommended that after an anodic oxidation process was finished, a negative voltage of, for example, -100 V to -200 V be applied in reverse for 0.1 hour to 5 hours. At this time, it is desirable that the temperature of the substrate is set at 100 °C to 250 °C, typically, at 150 °C. Mobile ions in the silicon oxide or at

the interface of the silicon oxide and the silicon were attracted by the gate electrode (Al) in this process.

[0034]

Then, boron was implanted into the silicon film 305 as an N-type impurity in a self-alignment manner by the ion doping method to form the source/ drain 308 and 309 of a TFT. Further, as shown in FIG. 2 (C), this was irradiated with the KrF laser light to improve the crystallization of the silicon film whose crystallization was degraded by doping the ions. At this time, the energy density of the laser light was set at 250 mJ/ cm^2 to 300 mJ/ cm^2. The sheet resistance of the source/ drain of this TFT became 300 Ω/ cm^2 to 800 Ω/ cm^2.

[0035]

Then, an interlayer insulating material 310 was formed of polyimide, and then a pixel electrode 313 was formed of ITO. Then, a contact hole was formed and electrodes 311 and 312 was formed of chromium/ aluminum multilayer film in the source/ drain region of the TFT, the one electrode 312 being connected also to the pixel electrode 313 made of ITO. The chromium/ aluminum multilayer film was made of an under chromium layer having a thickness of 20 Å to 2000 Å, here, 1000 Å, and an over aluminum layer having a thickness of 1000 Å to 20000 Å, here, 5000 Å. It is desired that these layers are formed in succession by the sputtering method. Lastly, they were annealed in hydrogen at 200 °C to 300 °C for 2 hours to finish

hydrogenating the silicon. In this way, a TFT was completed. Many TFTs manufactured at the same time were arranged in a shape of matrix to complete one substrate of the display portion of an active matrix type liquid crystal display device. Also in the present embodiment, the concentration of nickel in the crystalline silicon film was 10^{17} cm^{-3} to 10^{18} cm^{-3}.

[0036]

If the constitution of the embodiment 1 and the constitution of the embodiment 2 are adopted, nickel elements existing in the crystal silicon can be electrically solidified (gettering), which can prevent the nickel element from having bad effects on the device when the device is operating.

[0037]

Further, in the present embodiments described above, the PSG (Phosphosilicate Glass) film was used as a material for gettering, but in addition to the PSG film, a BSG film (Boron Silicate Glass) or a BPSG film can be used. Further, halogen elements (for example, chlorine) may be added to these films to improve a gettering effect. Still further, although the spin-coating method was used as a method of forming these films so as to ensure flatness, a vapor phase method may also be used.

[0038]

[Effects of the Invention] The PSG film was formed on the substrate, and then the under silicon oxide film was formed and then was crystallized by the nickel at the low temperature

(which means that the silicon oxide film was crystallized at the temperature lower than ever) to form the crystal silicon. This constitution of forming the crystal silicon could prevent the electrical characteristics of the semiconductor device utilizing this crystal silicon from being affected by the existing nickel.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 illustrates a manufacturing process of the embodiment.

[FIG. 2]

FIG. 2 illustrates a constitution of the embodiment.

[FIG. 3]

FIG. 3 illustrates a manufacturing process of the embodiment.

[Description of the Reference Numerals]

99-PSG film, 101-glass substrate, 102-PSG film, 103-mask, 104-silicon film, 105-direction of the growth of a crystal, 106-gate insulating film, 107-gate electrode, 108-anodic oxide layer, 109-gate electrode, 110-anodic oxide layer, 111-source/ drain region, 112-channel forming region, 113-drain/ source region, 114-source/ drain region, 115-channel forming region, 116-drain/ source region, 117-electrode, 118-interlayer insulator, 119-electrode, 120-electrode, 301-glass electrode, 302-PSG film, 303-underlayer film

(silicon oxide film), 304-silicon film, 305-gate insulating film, 306-gate electrode, 307-source/ drain region, 308-channel forming region, 309-drain/ source region, 310-interlayer insulator, 311-electrode, 312-electrode, 313-ITO (pixel electrode), 314-anodic oxide layer

FIG. 1-Laser light, FIG. 2-(Ni addition region)

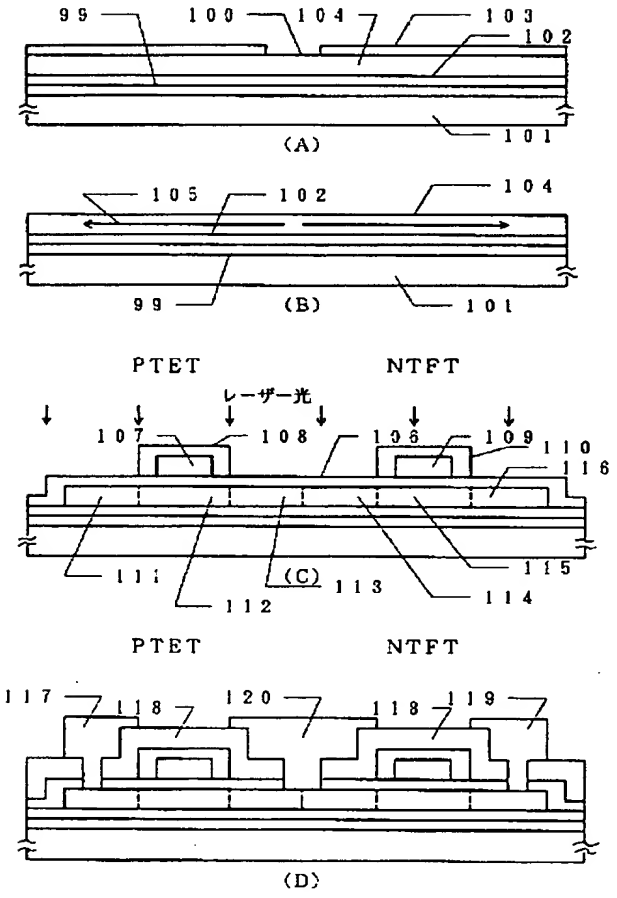
9

１１０	陽極酸化物層
１１１	ソース／ドレイン領域
１１２	チャネル形成領域
１１３	ドレイン／ソース領域
１１４	ソース／ドレイン領域
１１５	チャネル形成領域
１１６	ドレイン／ソース領域
１１７	電極
１１８	層間絶縁物
１２０	電極
１１９	電極
３０１	ガラス電極
３０２	ＰＳＧ膜

10

３０３	下地膜（酸化珪素膜）
３０４	シリコン膜
３０５	ゲイト絶縁膜
３０６	ゲイト電極
３０７	ソース／ドレイン領域
３０８	チャネル形成領域
３０９	ドレイン／ソース領域
３１０	層間絶縁物
３１１	電極
３１２	電極
３１３	ＩＴＯ（画素電極）
３１４	陽極酸化物層

【図１】



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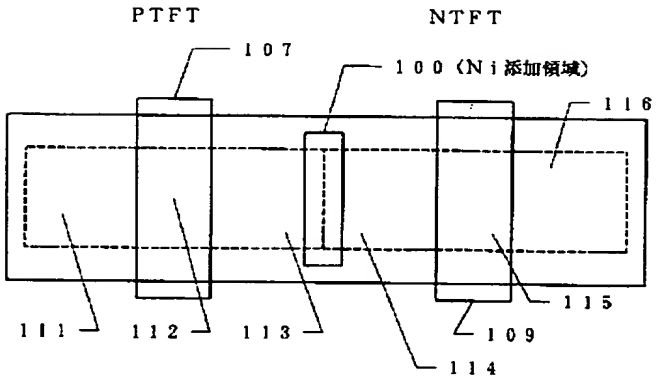

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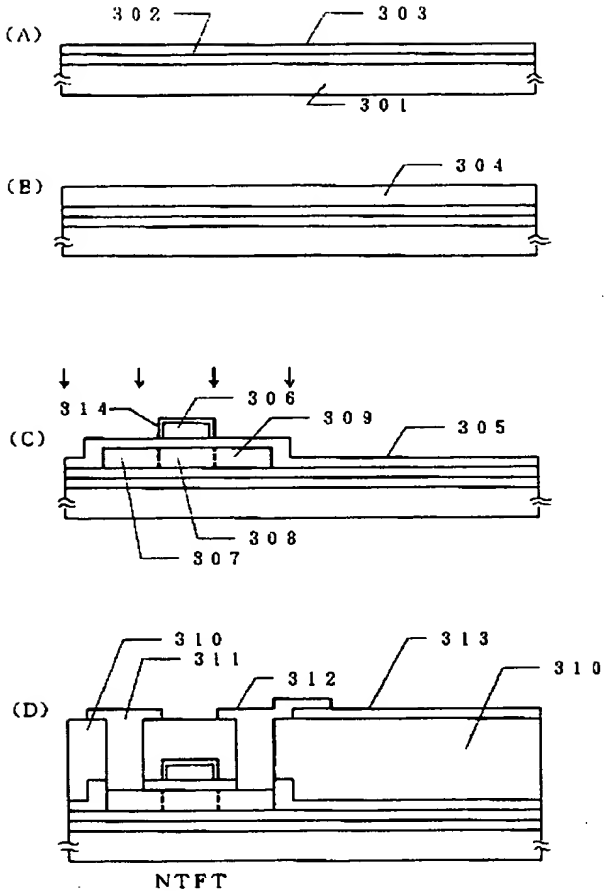

フロントページの続き

(51) Int. Cl.[5]	識別記号	庁内整理番号	Ｆ Ｉ	技術表示箇所
Ｈ０１Ｌ　29/784				